AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings includes changes to Figs. 1-5. These sheets, which includes Figs. 1, 2, 3A, 3B, 4A, 4B and 5, replace the original sheets including Figs. 1-5.

REMARKS/ARGUMENTS

Claims 1-42 stand rejected in the outstanding Official Action. Claims 1, 15, 22, 35 and 36 have been amended and therefore claims 1-42 remain in this application.

In section 2 on page 2 of the outstanding Official Action, the Examiner objects to the drawings and notes that Figures 1, 2, 3A, 3B, 4 and 5 should be designated "Prior Art." Applicant agrees and encloses herewith substitute sheets of drawings with the figures designated as "Prior Art." Additionally, the Examiner objects to Figure 4 as containing two figures. Figure 4 has been broken up into Figures 4A and 4B and the corresponding portions of Applicant's specification amended to reflect this division.

In view of the above replacement sheets and specification modifications, the drawings are believed to meet PTO requirements and notice to that effect is respectfully requested.

The title has been amended in accordance with the Examiner's suggestion.

Claims 15 and 36 are objected to because of a lack of antecedent basis for "the shift operation." Applicant has amended claims 15 and 36 to read as the Examiner assumes "a shift operation."

Claims 35-39 are objected to because claim 35 depends from claim 1 which is not a method claim. The Examiner correctly noted and the claim has now been amended to reference "the method of claim 22."

In view of the above amendments to the claims, it is submitted that claims 1-42 meet all requirements of 35 USC §112 (first paragraph).

Claims 1 and 22 stand rejected on page 4 of the Official Action under 35 USC §112 (second paragraph) as being indefinite. The Examiner indicates that claim 1's recitation of adding together "selected of said operands and said shifted operand" is indefinite. Applicant agrees and has amended claim 1 (and corresponding claim 22) to read "selected ones of said operands and said shifted operand." Thus, the claim positively recites what is being added together in dependence upon the instruction. Claims 1 and 22 have been amended to correct the language as noted.

Claims 1-42 stand rejected under 35 USC §102 as being anticipated by Applicant's Admitted Prior Art (Figures 1-5 and Description of Prior Art in the specification, pages 1-5). The Court of Appeals for the Federal Circuit has noted in the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) that "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

Applicant has modified the language in independent claim 1 so as to clearly specify in means-plus-function form the "address generation logic for receiving" and the "operand routing logic . . . for routing." Thus the claim positively recites the corresponding structure which performs the claimed functions. In order to anticipate Applicant's claimed invention, the burden is on the Examiner to demonstrate how or where the admitted prior art contains any teaching of these two positively recited structures in claim 1 or method steps in claim 22.

In order to understand and appreciate the difference between the prior art noted in Applicant's specification and the claimed invention, a synopsis of the background of Applicant's invention may be helpful. The claimed invention relates to generating an address in a data

processing apparatus. As discussed, several processes of generating addresses are well known, and there are various arrangements used in the past to generate such addresses as shown in Figures 3A, 3B, 4A, 4B and 5. In particular, often an address needs to be generated based upon a shift or an add operation. The noted prior art arrangements have partitioned these operations in different ways to try to improve the performance of the address generation stage.

In the arrangement shown in Figure 3A, the shift and add operation is performed by a single unit 120 in the pipeline. Thus, unit 120 is able to perform any shift left or right by any number of bits which may be required.

In Figure 4, two units are provided, the first of which provides a shift operation (unit 160) and the second of which then performs an add operation. Unit 160 is also able to perform any shift left or right by any number of bits which may be required.

In the arrangement shown in Figure 5, there are two logic units, one of which performs a shift operation (unit 160) and one of which performs an add operation. However, in Figure 5 there is also provided two multiplexers which enable the shift stage to be bypassed when required. As mentioned above, unit 160 is also able to perform any shift left or right by any number of bits which may be required.

The distinction with the above three different ways of accomplishing the desired result of address generation, is that in Applicant's claimed invention (as shown in Figure 6A), there is provided shift logic 216 which is able to perform any shift operation and add/shift logic 220 which is able to perform a predetermined shift operation, as well as an add operation. Thus, the basic difference between the prior art and the present invention is that in the present invention there is an add/shift logic 220 which performs a single predetermined shift operation as well as

the shift logic 216 which can perform any shift operation prior to an operand being provided to the add/shift logic 220. The idea of providing add/shift logic 220 which can perform a particular shift operation together with shift logic 216 which can perform all other shift operations prior to this being provided to the adder is not known from the prior art.

The above structures are characterized in Applicant's independent claim 1 by address generation logic for receiving operands, for generating a shifted operands and for adding together in dependence on instruction, "selected ones of said operands and said shifted operand to generate said address." Applicant's independent claim 1 also provides "operand routing logic . . . for routing operands . . . via operand manipulation logic for manipulation of said operands prior to routing to said address generation logic." Similar method steps are recited in method claim 22 corresponding to the structures accomplishing the above operations in means-plus-function form.

It becomes apparent from a detailed review of the Examiner's rejection under 35 USC §102 that the Examiner has taken selected features from three entirely different address generation arrangements and then combining those features as shown only in the present claim. This is clearly shown in reviewing the Examiner's arguments on page 5 in which he considers the disclosure in Figure 3B of Applicant's specification to be analogous to the "address generation logic"recited in Applicant's independent claim. However, at no point in Figure 3 or in the discussion of Figure 3 is there any disclosure of "operand routing logic . . . for routing operands . . . via operand manipulation logic for manipulation of said operands prior to routing to said address generation logic." Where such claimed operand routing logic is shown in any of Applicant's acknowledged prior art is not seen and clarification requested by the Examiner.

The Examiner then relies upon the prior art in Figure 4 which he contends is analogous to the claimed "operand manipulation logic." However, Figure 4 fails to disclose the claimed "address generation logic . . . for generating a shifted operand from one of said operands" as required by claim 1. It is noted that adder 140 in Figure 4 simply performs an add without any shift operation.

The Examiner then has to resort to the arrangement shown in Figure 5 of Applicant's specification to contend that multiplexers 165 and 155 are analogous to Applicant's claimed operand routing logic (as apparently contended by the Examiner in the third paragraph on page 6 of the Official Action), but this then fails to disclose the address generation logic as set out in claim 1 for the same reasons noted above.

While Applicant's Figures 3, 4 and 5 are three completely different ways to accomplish the desirable result of address generation, the Examiner has taken bits and pieces from each of these three and combined those bits and pieces in the manner disclosed only by Applicant's claim. There is no suggestion in the admitted prior art for parsing three different address generation schemes and combining bits and pieces of those schemes in the manner of Applicant's claim.

In accordance with the above, no individual embodiment of prior art address generation schemes discloses each element and each interrelationship of elements set out in Applicant's claim and therefore there is no basis for an anticipation rejection under section 102. At best, Applicant's admitted prior art includes the structures recited in Applicant's independent claim 1, but those structures are recited in three different embodiments, and there is no suggestion for

taking those elements out of their disclosed context and combining them in the manner of Applicant's independent claims 1 and 22.

As discussed in Applicant's specification on page 5, line 28 through page 6, line 10, Applicant's claimed arrangement enables one particular shift and add operation to be performed as fast as possible, and thus when the occurrence of these operations is high, it will be appreciated that this claimed invention can significantly improve the performance of the data processing apparatus. None of Applicant's admitted prior art embodiments contains any such problem recognition let alone a suggestion for combination of elements from the three Figures. Should the Examiner believe the discussion to include such suggestion, she is respectfully requested to identify that portion of Applicant's prior art disclosure.

Absent any indication that the admitted prior art contains any suggestion or motivation for choosing elements disclosed in three different embodiments and for combining them in the manner of Applicant's claim 1, there is no support for any rejection of independent claims 1 and 22 or claims dependent thereon under 35 USC §103, let alone §102, and any further rejection thereunder is respectfully traversed.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-42 are in condition for allowance and notice to that effect is respectfully requested. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, she is respectfully requested to contact Applicant's undersigned representative.

Respectfully submitted,

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